



## Asha Kumari Jakhar

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### Area of Interest

Machine learning-based surrogate modeling and uncertainty quantification for high-speed on-chip interconnects, particularly multilayer graphene interconnects; FinFET-driven repeater optimization for delay and signal integrity enhancement; neuro-inspired and metaheuristic optimization techniques (e.g., PSO) for interconnect-circuit co-design; integration of prior knowledge and physics-guided learning into compact modeling of nanoscale interconnect systems.

### Education

| Year | Degree/Examination       | Department & Specialization                             | Institution & Board                                                 | CGPA/Percentage |
|------|--------------------------|---------------------------------------------------------|---------------------------------------------------------------------|-----------------|
| 2025 | Ph.D. (viva 14-11-2025)  | Electronics & Communication and Microelectronics & VLSI | Indian Institute of Technology, Roorkee, India.                     | 8.143           |
| 2015 | Postgraduate (PG)        | Electronics & Communication, and Digital communication  | Sobhasaria Group of Institutions, Sikar(Raj.) & RTU Kota India.     | 71.50 %         |
| 2013 | Graduate (UG)            | Electronics & communication                             | Sobhasaria Group of Institutions, Sikar(Raj.) & RTU Kota India.     | 83.98 %         |
| 2009 | Intermediate (Class XII) | Physics, Chemistry, and Maths                           | Sikar Vidya Peeth Senior Secondary School, Sikar & RBSE India.      | 83.54 %         |
| 2007 | Matriculate (Class X)    | ALL                                                     | Shri BB Biyani Girls AVM SS Rishikul Marg,Sikar(Raj.) & RBSE India. | 85.50 %         |

### Ph.D. details

August 2020 - November 2025

**Title:** Enhanced Machine Learning Frameworks for Fast And Accurate Uncertainty Quantification and Repeater Optimization in Graphene-Based On-Chip Interconnects

**Research Interest:** Graphene and Carbon-Based on-chip interconnects (MLGNRs, MWCNTs), VLSI Interconnect Modeling and Optimization, Uncertainty Quantification (UQ) and ML-based Surrogate Modeling, High-Performance Computing (HPC) and Multiscale Simulation for Electronic Design Automation (EDA), AI/ML Applications in Semiconductor Device and Interconnect Design

### M. Tech details

October 2013 - December 2015

**Title:** performance analysis of AODV, DSR, OLSR, GRP and TORA with FTP and HTTP Load in MANET on OPNET Simulator

**Dissertation:** This dissertation presents a comparative analysis of five MANET routing protocols: AODV, DSR, OLSR, GRP and TORA, using OPNET 14.5 simulation software. The performance of these protocols is evaluated for different node groups (20, 40 and 60 nodes) based on parameters such as delay, throughput, load, bits transmitted and bits received using IEEE 802.11g standard. The study aims to identify the most efficient routing protocol for reliable and better communication in MANET environments.

### Experience

**Post Doctoral :** IISC Bengaluru under Prof. Mayank Shrivastava for ML based device failure modeling.

**Assistant Professor** | Swami Keshvanand Institute of Technology Management & Gramothan Jaipur, Rajasthan 302017, INDIA

August 2016 - December 2017

- Teaching undergraduate courses such as Analog Electronics, Digital Electronics, Network Analysis and Synthesis and Communication Systems.
- Conducted the undergraduate labs like Digital Electronics Lab, Basic Electronics Lab, and Analog Circuit Lab.

### Internships

**Basics of Telecom Network** | Bharat Sanchar Nigam Limited, Sikar (Rajasthan)

June 2012 - July 2012

- I gained hands-on experience with telecom network technologies, including GSM, fiber optics, and broadband systems. This training covered both theoretical aspects and practical exposure to network infrastructure and operations.

### B. Tech Projects

**Interfacing Color Sensor with Microcontroller**

June 2012 - Dec 2012

Designed a color detection system using LDR and RGB LEDs interfaced with an AT89S52 microcontroller and ADC0808. The system measures light reflectance to identify colors and display them on an LCD, demonstrating real-time optical sensing for automation and data encoding applications.

Designed a self-defense device that delivers a safe electric shock and sends an SMS alert to pre-stored contacts. The system integrates an astable multivibrator (1 kHz), inverter circuit, voltage quadrupler, and step-up transformer (9V to 200V, 500 mA). An auto-SMS module triggers alerts during activation, enhancing real-time personal safety without requiring a firearm license.

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### **Awards / Scholarships / Academic Achievements**

- GATE Qualified (2020): Successfully cleared the Graduate Aptitude Test in Engineering
- GATE Qualified (2019): Successfully cleared the Graduate Aptitude Test in Engineering
- UGC NET for assistant professor qualifies in 2015.
- UGC NET for assistant professor qualifies in 2017.
- UGC NET JRF (2019): Qualified for the Junior Research Fellowship.

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### **Skills**

**Computer languages:** MATLAB: Extensive experience in modeling and analysis of HSPICE outputs, data processing, and algorithm development. Python: Skilled in data analysis, machine learning, and ANN training.

Proficient in using Python libraries such as NumPy, pandas, scikit-learn, and TensorFlow/Keras for scientific computing, data processing, and neural network implementations.

**Software Packages:** 1. HSPICE: Extensive experience in high-speed on-chip interconnect modeling, including Multi-Layer Graphene Nanoribbon (MLG NR) and signal integrity analysis. Skilled in performing non-linear analysis such as eye diagram characteristics to evaluate signal performance and integrity. Lumerical: Proficient in optical interconnect modeling, including designing and analyzing half-ring resonators. Experienced in evaluating coupling efficiency and coupling length to optimize optical communication performance.

2. TCAD: Basic diode I-V characteristics analysis. 3. CADENCE Virtuoso: schematic and layout design and delay analysis for CMOS inverters.

**Languages Known:** ENGLISH, SPANISH, Hindi, Marwari

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### **Research Publications**

#### **Journals**

- A. K. Jakhar, R. Sharma, A. Dasgupta and S. Roy, "A Neural Network Guided Approach for Repeater Optimization in Multilayer Graphene On-Chip Interconnect Networks Including TSVs," in *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, doi: 10.1109/JMMCT.2025.3625423.
- Surila Guglani, Asha Kumari Jakhar, Km Dimple, Ankit Sukhija, Avirup Dasgupta, Rohit Sharma, Brajesh Kumar Kaushik, and Sourajeet Roy, "Artificial Neural Networks With Fast Transfer Learning for Statistical Signal Integrity Analysis of MWCNT and MLG NR Interconnect Networks", in *IEEE Transactions on Electromagnetic Compatibility*, IEEE, 2024
- Surila Guglani, Asha Kumari Jakhar\*, Avirup Dasgupta, and Sourajeet Roy, "Combining Prior Knowledge with Transfer Learning (PKID-TL) for Fast Neural Network Enabled Uncertainty Quantification of Graphene On-Chip Interconnects", in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, IEEE, 2024.

“\*” :- Equally contributed.

#### **Conferences**

- Asha Kumari Jakhar, Dyuti Basu, Km Dimple, Surila Guglani, Avirup Dasgupta, and Sourajeet Roy, "A Fast Metalearning Algorithm for Neural Network Enabled Uncertainty Quantification of Graphene Based Interconnects with Passive Shielding", in *EMC 2024 / IEEE Symposium on EMC, SI & PI in Phoenix, AZ*, IEEE, 2024
- Asha Kumari Jakhar, Surila Guglani, Avirup Dasgupta, and Sourajeet Roy, "Prior Knowledge Accelerated Transfer Learning (PKI- TL) for Machine Learning Assisted Uncertainty Quantification of MLG NR Interconnect Networks", in *2023 IEEE 32nd Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, IEEE, 2023
- Asha Kumari Jakhar, Surila Guglani, Avirup Dasgupta, and Sourajeet Roy, "Noise-Aware Uncertainty Quantification of MLG NR Interconnects using Fast Trained Artificial Neural Networks", in *IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)*, IEEE, 2023.
- Asha Jakhar, Rohit Sharma, Avirup Dasgupta, and Sourajeet Roy, "Spacer Optimization using a Neuro-PSO Approach for Improving FinFET Repeater Performance in On-Chip Global MLG NR Interconnects", in *IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)*, IEEE, 2024.

#### **References**

1. Dr. Sourajeet Roy (Associate Professor) IIT Roorkee

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2. Dr. Rohit Yogendra Sharma (Professor) IIT Ropar

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3. Dr. Avirup Dasgupta (Associate Professor) IIT Roorkee

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