Jawaharlal Nehru University

One Day workshop on VLSI Design using Cadence Tools

Jointly organized by

School of Computer & Systems Sciences and School of Engineering

Agenda

Registration: 09:30 am. to 10:00 a.m.

Inauguration by Chief Patron Prof.Santishree Dhulipudi Pandit (V.C., JNU)
(09:40 a.m to 9:45 a.m) Venue: (Seminar Hall, SC&SS)

Inaugural talk by Dean of SC&SS and SOE (09:45 a.m. to 09.50 a.m.)

Introduction by Chief Investigator and Co-Investigator of C2S Program at JNU
(09:50 a.m. to 10:00 a.m.) Venue: (Seminar Hall,SC&SS)

Morning Session (10:00 a.m. to 01:00 p.m.) Venue : Computer Lab, SC&SS/Computer Lab, SOE, JNU

Speaker 1

Session by Entuple

- Introduction to Semi Custom IC Design Flow
- Cadence Solutions for Semi Custom IC Design
- Functional Verification using INCISIVE
- RTL Synthesis using GENUS Synthesis Solution
- Reports Generation (Power, Timing and Area)

Lunch (01:00 p.m. to 02:00 p.m.)

Afternoon session (02:00 p.m to 05:30 p.m) Venue: Computer Lab, SC&SS/ Computer Lab, SOE, JNU

- Physical Implementation using INNOVUS that includes
- Floor Planning
- Power Planning
- Placement
- CTS
- Routing
- Generation of GDSII

Speaker 2

Speaker 3

Vote of Thanks by Convenor. 5.30 p.m.

Tea Time: 5:35 p.m.

Limited seats are available

Registraion:https://forms.gle/s5vn5knYJmginVsY9

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www.c2s.gov.in

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